Amendments to the Specification:

Please correct the paragraph beginning on line 7 of Page 3, as follows:

Fig. 6(a) is a diagram showing how the channel body of the transistor is charged during a write ~~A~~"1" operation, and Fig. 6(b) is a diagram showing how this channel body is discharged during a write ~~A~~"0" operation.

Please correct the paragraph beginning on line 2 of Page 4, as follows:

Fig. 2 is a diagram showing a first type of DRAM gain cell having a floating-body structure. The cell is formed from a single transistor having a source S connected to a reference potential RP (e.g., ground), a drain D connected to a bit line, and a gate G connected to a word line. A diode DD is provided to show a direction in which the drain junction is forward biased during a write ~~A~~"0" operation, and a current source CS is provided to show the direction in which impact ionization current flows when the transistor operates in a saturated operating region (i.e., when the drain voltage is greater than the gate voltage minus the threshold voltage, $V_g - V_T$) during a write ~~A~~"1" operation. As will become more apparent below, DD and CS are inherent to the transistor structure and are shown in Fig. 2 for explanatory purposes only.

Please correct the paragraph beginning on line 5 of Page 6, as follows:

To write data in the cell, the body is either discharged by forward biasing the drain-to-body diode or charged by impact ionization current, respectively shown as DD and CS in the equivalent circuit diagram of Fig. 2. That is, to write ~~A~~"1" in the cell, the word line is asserted

and then charge is pumped into the body by impact ionization current created by voltage on the bit line. Conversely, to write a ~~A~~"0" in the cell, the word line is reduced in voltage and the channel body is discharged when the drain diode is forward biased. A more detailed explanation of the internal operation of the cell during a write operation will now be given.

Please correct the paragraph beginning on line 20 of Page 6, as follows:

When the gate voltage falls below its threshold and the bit line assumes a digital ~~A~~"0" value, the pn junction between the drain and the silicon layer is forward biased; that is, the body-to-drain diode DD is turned on. As a result, the holes in the body flow to the drain side of the transistor, thereby causing the body to develop a charge corresponding to digital data ~~A~~"0". The migration of holes to the drain side which produces this cell state is shown in Fig. 6(b).

Please correct the paragraphs beginning on lines 3, 10, and 14 of Page 7, as follows:

A digital ~~A~~"1" or ~~A~~"0" is therefore stored as a difference in the potential of the channel body. As shown in Fig. 7, when the channel body assumes a higher potential V_{T1} due to hole accumulation, the cell assumes a digital ~~A~~"1" state. And, when the channel body assumes a lower potential V_{T0} due to the absence of holes, the cell assumes a digital ~~A~~"0" state. Here, V_{WL} corresponds to the word line voltage connected to the gate. Note that when the cell is in a "1" state, the threshold voltage is lower than when in the "0" state; that is, $V_{T1} < V_{T0}$. Thus, the current of the cell in a "1" state is higher than when in a "0" state through the body effect.

In order to hold the ~~A~~"1" in the cell, a negative bias voltage may be applied to the word

line to hold the accumulation of holes in the channel body. In theory, this data hold state is not changed even when a read operation is performed, as long as the read operation is performed in a linear region unless a write operation of inverted data (erase operation) is performed.

To read data from the cell, the body effect modulates the on-state current of the transistor. By detecting this current, the cell state (e.g., stored data), which is determined by the potential stored in the body, may be sensed. A read operation may therefore be performed by detecting a difference in bit line current when the bit line is clamped at a predetermined potential. The difference in bit line current under these conditions will determine whether a ~~A~~"1" or ~~A~~"0" is stored in the cell.

Please correct the paragraph beginning on line 11 of Page 8, as follows:

Second, when implemented using bulk silicon in a memory array, retention time of the floating body cell is extremely short because unselected cells suffer severe disturbs during a write operation. For example, a cell storing a digital ~~A~~"1"value partially discharges when another cell in the same column is written with a digital value of "0." Consequently, the cell storing the partially discharged ~~A~~"1"loses its state much sooner, which means it has a shorter retention time. These effects have been may be undesirable when attempting to construct a performance-efficient memory.

Please correct the paragraph beginning on line 1 of Page 9, as follows:

An equivalent circuit diagram of the second type of cell is shown in Fig. 9. This diagram includes a virtual diode 140 which shows a direction in which the source junction is forward biased during a write ~~A~~"0" operation, and a virtual current source 150 which shows the direction in which impact ionization current flows when the write word, word, and bit lines are set to predetermined values during a write ~~A~~"1" operation. The diode and current source are inherent to the transistor structure and are shown in the equivalent circuit diagram for explanatory purposes only.

Please correct the paragraphs beginning on line 12 of Page 9 and lines 3 and 8 of Page 10 as follows:

To write data in the cell, the channel body of the transistor is either charged by impact ionization current or discharged by forward biasing the source-to-body diode. To write a digital value of ~~A~~"1" in the cell, the word and write word lines are asserted; that is, both word lines are raised to predetermined voltage states. This causes capacitive coupling to occur between the gate and channel body and also impact ionization current to flow, which results in charging the channel body of the transistor. More specifically, raising the voltage of the write word line causes impact ionization current to flow from an area near the drain into the channel body. As a result, holes produced by the impact ionization current migrate as majority carriers into the body, thereby charging the body to a potential which corresponds to a digital data value of "1." Unlike

the Fig. 2 cell, the impact ionization current is therefore generated when the word and write word lines are asserted during a write ~~A~~"1" operation. (The source/write word line may therefore be said to act like a drain under these circumstances.)

To write a digital value of ~~A~~"0" in the cell, the voltage of the bit line is lowered to a value which is preferably below ground. This causes the virtual diode to become forward biased; that is, the channel body discharges when the holes migrate from the body to the source side of the transistor. The body therefore develops a charge (or lack thereof) which corresponds to a digital value of "0."

To read data from the cell, the aforementioned technique may be used. This involves detecting a difference in bit line current (caused by the body effect) when the bit line is clamped at a predetermined potential. The difference in bit line current under these conditions will determine whether a ~~A~~"1" or ~~A~~"0" is stored in the cell.

Please correct the paragraph beginning on line 20 of Page 10, as follows:

In the second stage, the cells which are to store a digital ~~A~~"0" are selectively altered by changing the voltages on their associated bit lines. For example, if a ~~A~~"0" value is to be stored in cell 206 but the value of ~~A~~"1" is to be retained in cell 205, the voltage on bit line 204 is lowered to a value below ground ("very low" in the chart) but the voltage on bit line 203 is maintained at "low." As a result, the body-to-source diode in cell transistor 206 becomes forward biased, thereby discharging the channel body in this transistor until the cell assumes a "0" value. Because

the voltage of bit line 203 does not change (i.e., remains at "low") during this time, the write "0" operation performed on cell 206 does not affect cell 205. As a result, cell 205 retains storage of its "1" value and cell 206 stores a "0" value. The voltage of write word line 202 may transition to "low" (e.g., ground) and word line 201 transitions to "medium" or "low" during this time. This two-stage write process is then performed for row 210 and subsequent rows until all cells in the array have been written with appropriate values.